FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 500987.02	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Daniel B. Penney	
		FILING DATE Concurrently herewith	GROUP ART UNIT Not Yet Assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
NTN	AA	5,021,688	06/04/91	Leforestier et al.	307	463	
NTN	AB	5,592,434	01/07/97	Iwamoto et al.	365	233	
NTN	AC	5,781,497	07/14/98	Patel et al.	365	230.06	
NTN	AD	5,825,714	10/20/98	Kohno	365	230.06	
NTN	AE	5,881,017	03/09/99	Matsumoto et al.	365	230.04	
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AK							
	AL							
	AM							
	AN							
	AO							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

NTN	AP	Choi, Y. et al., "16-Mb Synchronous DRAM with 125-Mbyte/s Data Rate", IEEE Journal of Solid-State Circuits, Vol. 29, No. 4, April 1994, pp. 529-533.
NTN	AQ	Sunaga, T. et al., "A Full Bit Prefetch Architecture for Synchronous DRAM's", IEEE Journal of Solid-State Circuits, Vol. 30, No. 9, September 1995, pp. 998-1005.

EXAMINER	Nam Nguyen	DATE CONSIDERED	2/27/04

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).